

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/750,423	12/30/2003	David Qiang Meng	10559-914001 / P16854	4620	
20985 FISH & RICHA	7590 02/01/2008 ARDSON, PC		EXAMINER		
P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			RUTZ, JARED IAN		
WINNEAFOLIS, WIN 33440-1022			ART UNIT	PAPER NUMBER	
			· 2187	· · · · · · · · · · · · · · · · · · ·	
			MAIL DATE	DELIVERY MODE	
			02/01/2008	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



UNITED STATES DEPARTMENT OF COMMERCE U.S. Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450

APPLICATION NO./	FILING DATE	FIRST NAMED INVENTOR /	ATTORNEY DOCKET NO.
CONTROL NO.		PATENT IN REEXAMINATION	

10750423

12/30/2003

MENG, DAVID QIANG

10559-914001 / P16854

FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022 EXAMINER

Jared I. Rutz

ART UNIT PAPER

2187 20080122

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The reply brief filed 11/19/2007 has been entered and considered. Please find attached a Supplemental Examiner's Answer addressing the new issues raised by said reply beief.

Supplemental Examiner's Answer

Responsive to the reply brief under 37 CFR 41.41 filed on 11/19/2007, a supplemental Examiner's Answer is set forth below:

Appellant's Reply Brief submitted 11/19/2007 has been noted by the Examiner.

The Reply Brief raises new issues not presented in the Appeal Brief submitted 6/18/207.

Accordingly, this Supplemental Examiner's Answer is submitted to address the new issues raised in said Reply Brief.

In the second and third paragraph beginning on page 8 of the Reply Brief submitted 11/19/2007, Appellant argues:

"Nevertheless, the Examiner mistakenly assumes that some huge 'modification to a known prior art CAM would be necessary to implement the claimed invention.' Rather, the modification needed to distinguish the Handy CAM from claim 1 is to configure the CAM with the partitions by the CAM manager, as pointed out above.

The ability to be partitioned into two groups of entries as recited in the claims results from a combination of the CAM manager and the functional aspects of a CAM. There are not modifications required to the CAM, but rather configuration by the CAM manager of the CAM and partition of the entries according to, e.g., IP and MAC addresses as mentioned above and as clearly discussed in the specification, as argued above."

10/750,423 Art Unit: 2187

Insofar as it is clear, Appellant would have the Board believe that the mere partitioning of a CAM is sufficient to provide "a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel" as recited in claim 1. Assuming arguendo that this were true, the Examiner respectfully points out that the invention recited in claims 21-26 would be anticipated by a prior art network device utilizing a prior art CAM as taught by Handy, as they would only differ from the claimed invention as to the arrangement of non-functional descriptive material, IP and MAC addresses.

However, as is evidenced by Appellant's submitted "Content-addressable memory" article, this is not the case. As stated in the second paragraph on page 1 of "Content-addressable memory":

"Unlike standard computer memory (random access memory or RAM) in which the user supplies a memory address and the RAM returns the data word stored at that address, a CAM is designed such that the user supplies a data word and the CAM searches its entire memory to see if that data word is stored anywhere in it. If the data word is found, the CAM returns a list of one or more storage addresses where the word was found (and in some architectures, it also returns the data word, or other associated pieces of data). Thus, a CAM is the hardware embodiment of what in software terms would be called an associative array."

This section clearly shows that in a conventional CAM, the entire memory is searched to locate the requested data word. This is also supported by pages 14-15 of

10/750,423 Art Unit: 2187

the Handy reference. With respect to the Handy reference, specifically figure 1.7, consider an implementation of a CAM having 10 registers and the comparator associated with each register. It would be within the ability of one of ordinary skill in the art to place one type of data in entries 1-5 and a second type of data in entries 6-10. However, when a user supplies a data word, identified as the compare address in figure 1.7 of Handy, that data would be compared to each data word stored in registers 1-10, and accordingly would not provide a first group of memory entries selectable independent of a second group of memory entries as required by independent claim 1. The Specification of the instant Application provides no guidance on how the disclosed invention allows a first group of entries that are accessible in parallel to be selectable independent of a second group of entries that are accessible in parallel.

In the second paragraph beginning on page 8, Appellant argues: "a CAM is a memory device and that it is a specialized memory that is implemented by RAM." The Examiner respectfully notes that the Specification of the instant Application does not state that the CAM may be implemented in RAM. Furthermore, Appellant's submitted "Content-addressable memory" article shows that such an embodiment would not satisfy the recited limitation "a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel". As stated in the fourth paragraph beginning on page 1 and the first paragraph beginning on page 2 of "Content-addressable memory":

10/750,423 Art Unit: 2187

"Because a CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all search applications. There are cost disadvantages to CAM however. Unlike a RAM chip, which has simple storage cells, each individual memory bit in a fully parallel CAM must have its own associated comparison circuit to detect a match between the stored bit and the input bit. Additionally, match outputs from each cell in the data word must be combined to yield a complete data word match signal. The extra circuitry also increases power dissipation since every comparison circuit is active on every clock cycle. Consequently, CAM is only used in specialized applications where searching speed cannot be accomplished using a less costly method."

"To achieve a different balance between speed, memory size, and cost, some implementations emulate the function of CAM by implementing standard tree search or hashing designs in hardware, using hardware tricks like replication or pipelining to speed up effective performance. These designs are often used in routers."

The Examiner respectfully submits that if, arguendo, the Specification of the instant Application had disclosed emulating a CAM using RAM, it would not be sufficient to teach the limitation "a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel". As CAM emulated with a RAM requires traversing a tree or generating a hash function to look up entries, it clearly does not teach that a group of entries are accessible in parallel.

10/750;423 Art Unit: 2187

With respect to Appellant's submitted "Partition (database)" article, the Examiner respectfully submits that it is not germane to the claimed invention. The submitted article is clearly directed to partitioning the tables of a database, and has nothing to do with partitioning a memory device to obtain "a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel".

With respect to Appellant's submitted "Content-Addressable Memory v5.1", it is unclear what Appellant considers relevant from this document. There does not seem to be any discussion of partitioning a memory device. With respect to this document's teaching regarding ternary mode, the Examiner respectfully notes that a CAM operating in ternary mode does not prevent any entry or subentry from being accessed, it merely makes the result of the comparison of selected bits of an entry not considered when determining if an entry matches the input data.

Accordingly, the Examiner maintains that the Specification of the instant

Application does not provide either an enabling disclosure for the invention as recited in

claims 1-26, nor does it describe the claimed invention in sufficient detail that one skilled

in the art can reasonably conclude that the inventor had possession of the claimed

invention.

10/750,423

Art Unit: 2187

Page 6

Appellant may file another reply brief in compliance with 37 CFR 41.41 within two

months of the date of mailing of this supplemental examiner's answer. Extensions of

time under 37 CFR 1.136(a) are not applicable to this two month time period. See 37

CFR 41.43(b)-(c).

Respectfully submitted,

Jared Rutz

ot

A Technology Center Director or designee has approved this

supplemental examiner's answer by signing below:

lmane Sha

Conferees:

Denald Sparks

DONALD SPARKS

SUPERVISORY PATENT EXAMINER

Mano Padmanabhan